

FIG. 1 (PRIOR ART)

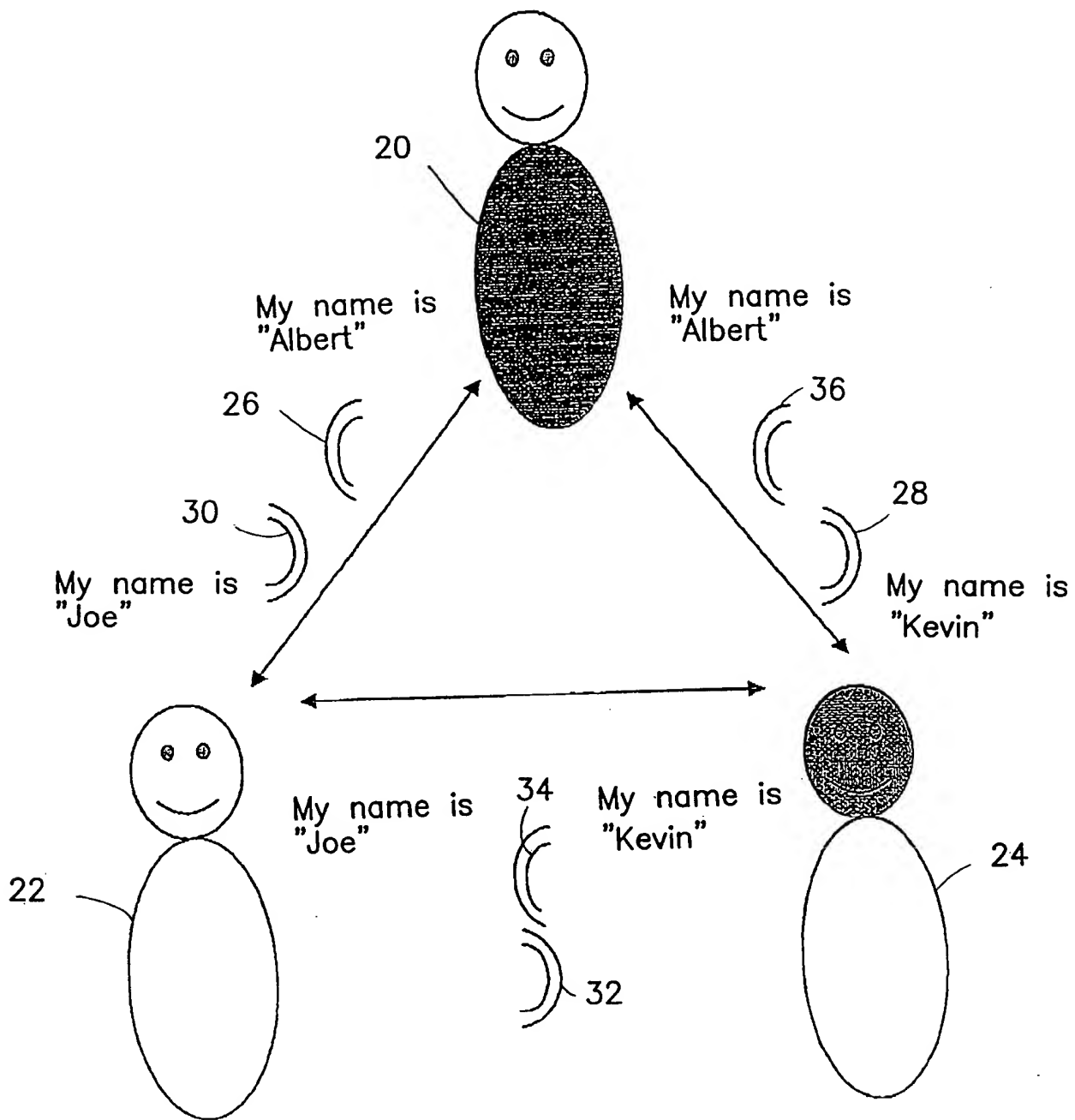


FIG. 2A

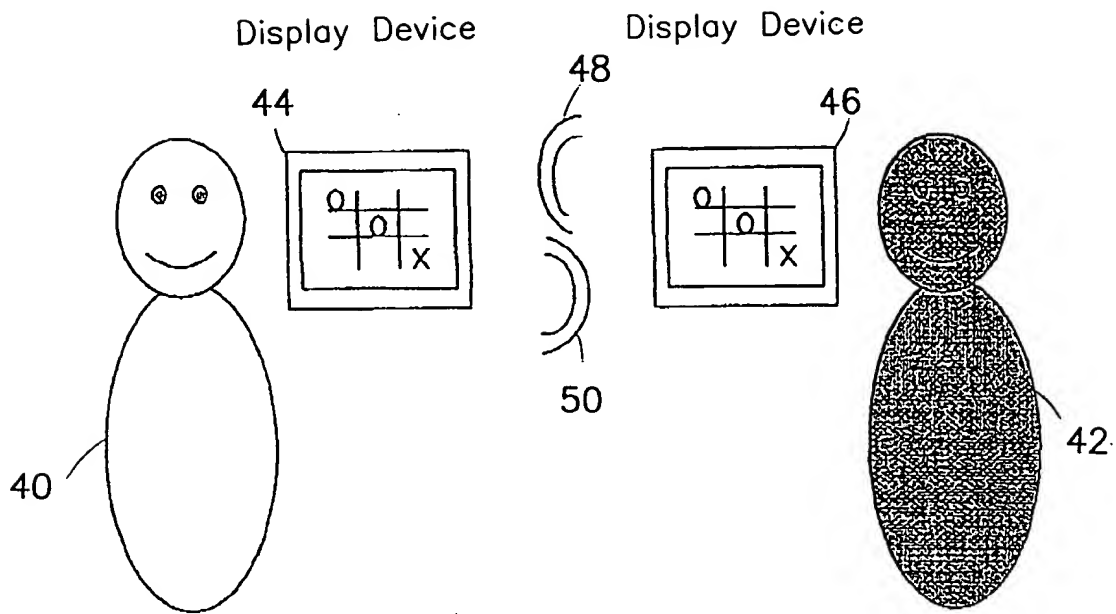


FIG. 2B

Original Digital Signal

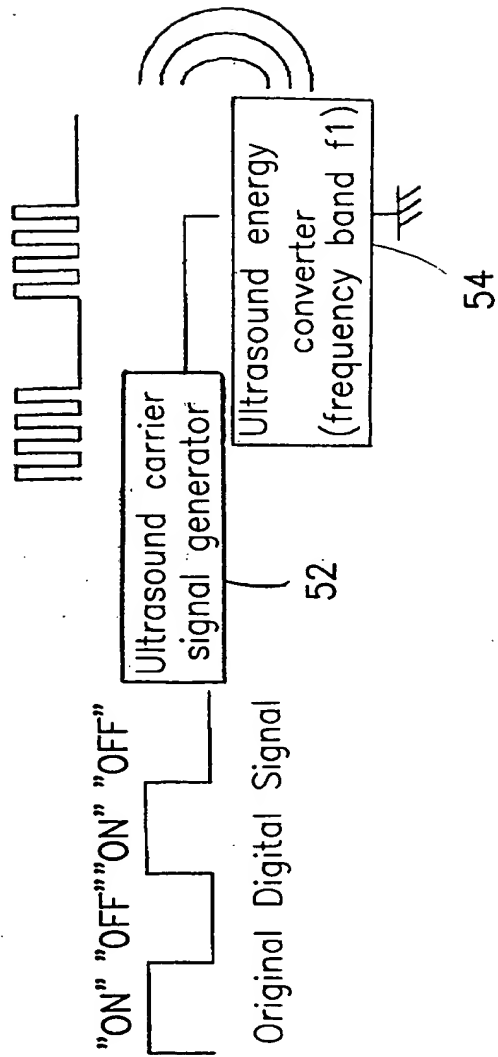


FIG. 3

FIG. 4A is a block diagram of a system for processing an amplified signal. The system includes an ultrasound energy converter (frequency band f1) 56, an amplifier circuit 58, and a fixed interval sampling circuit 60. The output of the sampling circuit 60 is an output signal series "0" "1" "0" "1".

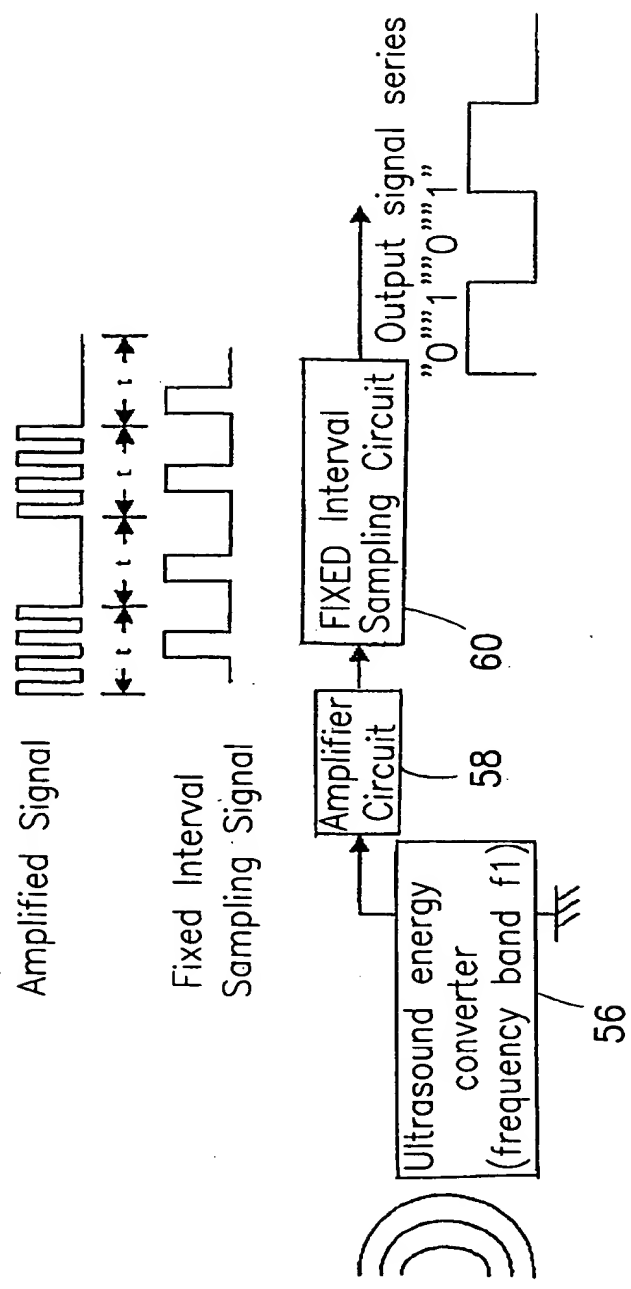


FIG. 4A

FIG. 4B is a block diagram of a system for processing an input signal. The system includes an input signal source 60, an amplifier circuit 64, an envelope detection circuit 66, and an output signal series 68. The input signal source 60 provides an input signal to the amplifier circuit 64. The amplifier circuit 64 amplifies the input signal and provides an amplified signal to the envelope detection circuit 66. The envelope detection circuit 66 detects the envelope of the amplified signal and provides an output signal series 68. The output signal series 68 is a series of pulses, each representing a detected envelope. The pulses are labeled "0" and "1", indicating a binary output signal.

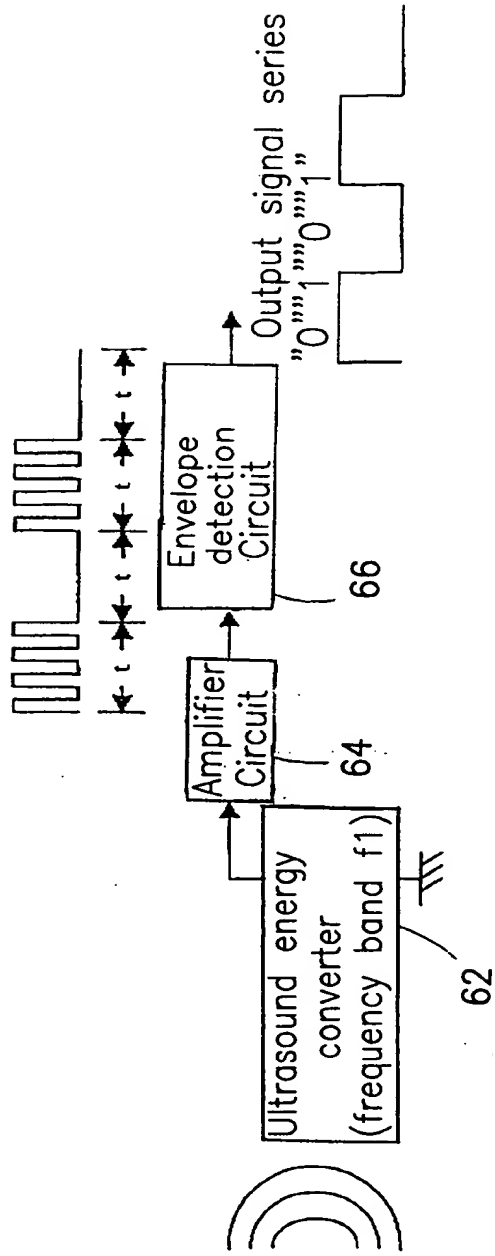


FIG. 4B

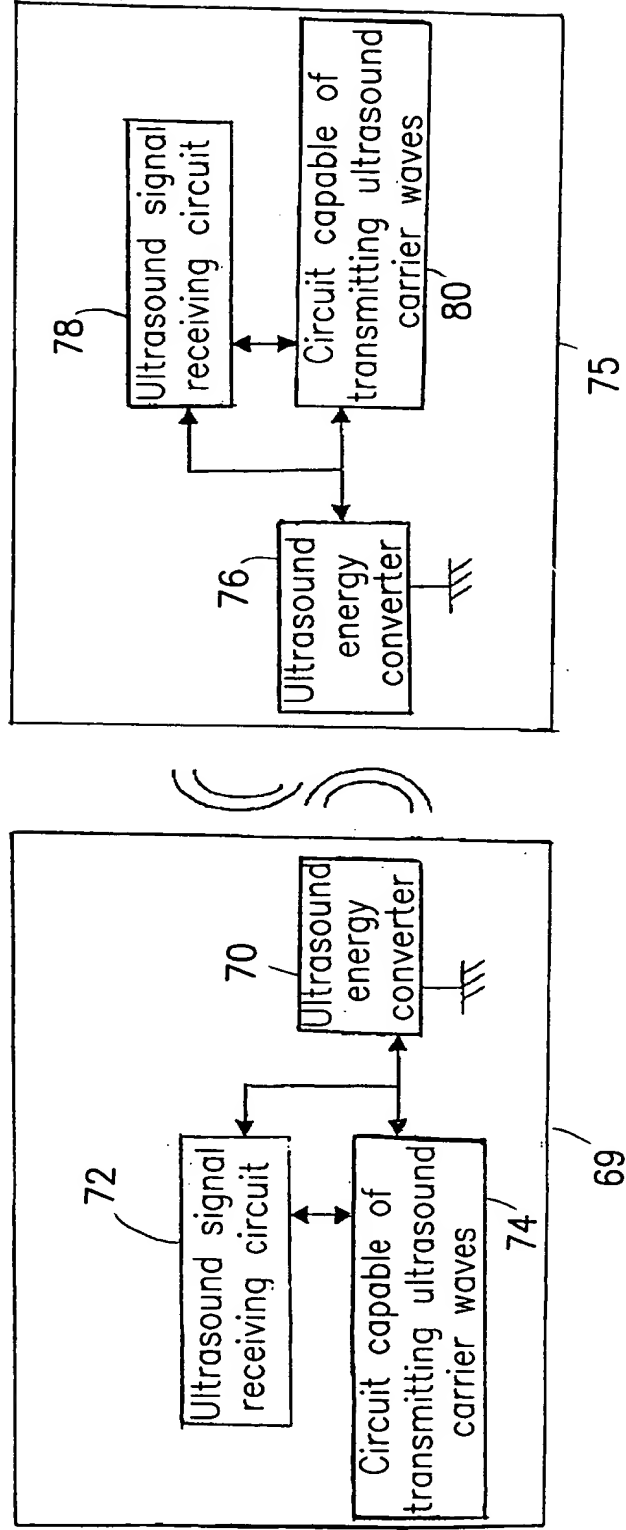


FIG. 5